

WHAT IS CLAIMED IS:

- 5 *Sub A2*
1. A method of controlling a power saving operation for a phase comparator unit, comprising the steps of:
- 10 dividing a frequency of a reference signal to generate a reference frequency divided signal;
- dividing a frequency of an input signal to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;
- 15 comparing the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;
- generating a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal;
- 20 generating a first initializing signal for initializing the output of the step of dividing the frequency of the reference signal in accordance with the power saving state canceling signal; and
- 25 generating a second initializing signal for initializing the output of the step of dividing the frequency of the input signal in accordance with the power saving state canceling signal.
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- 35 2. The method as claimed in claim 1, wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and

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a first initializing signal generator
which generates a first initializing signal for

a second initializing signal generator
5 which generates a second initializing signal for
initializing the comparison signal frequency
dividing unit in accordance with the power saving
state canceling signal.

6. The PLL frequency synthesizer as claimed in claim 5, wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other.

7. A semiconductor integrated circuit including a PLL frequency synthesizer comprising:
a phase comparator unit;
a loop filter which receives an output of the phase comparator unit; and
a voltage control oscillator which receives an output of the loop filter,
the phase comparator unit comprising:
a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal;
a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency

divided signal;

a phase comparator which compares the
phases of the reference frequency divided signal and
the comparison frequency divided signal so as to
5 output a comparison result;

a canceling signal generator which
generates a power saving state canceling signal in
accordance with the reference frequency divided
signal and the comparison frequency divided signal;

10 a first initializing signal generator
which generates a first initializing signal for
initializing the reference signal frequency dividing
unit in accordance with the power saving state
canceling signal; and

15 a second initializing signal generator
which generates a second initializing signal for
initializing the comparison signal frequency
dividing unit in accordance with the power saving
state canceling signal.

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8. The semiconductor integrated circuit
25 as claimed in claim 7, wherein frequency dividing
rates used in the reference signal frequency
dividing unit and in the comparison signal frequency
dividing unit can be set independently of each other.

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9. A transmitter-receiver including a PLL
frequency synthesizer comprising:

35 a phase comparator unit;

a loop filter which receives an output of
the phase comparator unit; and

a voltage control oscillator which receives an output of the loop filter,

the phase comparator unit comprising:

a reference signal frequency dividing unit
5 which divides a frequency of a reference signal to generate a reference frequency divided signal;

a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison
10 frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;

a phase comparator which compares the phases of the reference frequency divided signal and
15 the comparison frequency divided signal so as to output a comparison result;

a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided
20 signal and the comparison frequency divided signal;

a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state
25 canceling signal; and

a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving
30 state canceling signal.

35 10. The transmitter-receiver as claimed in claim 9, wherein frequency dividing rates used in the reference signal frequency dividing unit and in

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the comparison | signal frequency dividing unit can be
set independently of each other.

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